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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
SCHILLINGER, LAURA M	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 09/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/023,347	HAUSE ET AL.	
	Examiner	Art Unit	
	Laura M. Schillinger	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-2, 4-8,10-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Yoshimura (WO 200167509 A).

The citations made below pertain to the US Application 2004/0135226 which claims priority to the WO 200167509 A document:

In reference to claim 1, Yoshimura teaches a method comprising:

Providing a wafer comprised of a bulk substrate (Fig.5a (21a)), an insulating layer positioned above the bulk substrate (Fig.1 (21b)) and a semiconducting layer positioned above the insulating layer (Fig.5a (21c)- SOI substrate 20);

Forming an opening in the semiconductor layer and the insulating layer to thereby expose a surface area of the substrate (Fig.5a)

Forming an alignment mark in the substrate within the exposed surface area of the substrate (Fig.52 (21c and 21d)) and

Forming a layer of material above the alignment mark in the opening (Fig.5f (26)).

In reference to claim 2, Yoshimura teaches wherein the wafer is comprised of silicon, and the semiconducting layer is comprised of silicon (page 5 [0062]).

In reference to claim 4, Yoshimura teaches wherein forming the opening comprises at least one etching process (page 5 [0063]).

In reference to claim 5, Yoshimura teaches wherein forming the alignment mark comprises:

Forming a patterned layer of photoresist above the exposed substrate area; and

Performing at least one etching process to form the alignment mark in the exposed area using the photoresist as a mask (Fig.5a and 5e and [0063-0065]).

In reference to claim 6, Yoshimura teaches wherein forming a layer of material above the alignment mark comprises depositing a layer above the alignment mark and in the opening (Fig.5E (26)).

In reference to claim 7, Yoshimura teaches wherein the material comprises at least one of silicon nitride or oxide and a material having a dielectric constant less than 8.0 (page 5, [0066]).

In reference to claim 8, Yoshimura teaches further comprising performing a planarization operation after forming the material above the alignment mark (Fig.5g (26 [0068]).

In reference to claim 10, Yoshimura teaches wherein forming the opening comprises forming a plurality of openings in the semiconducting layer and the insulating layer (Fig.5E (21c and 21d).

In reference to claim 11, Yoshimura teaches wherein forming the alignment mark comprises forming an alignment mark in the substrate within the exposed area of each opening (Fig.5E (21c and 21d)).

In reference to claim 12, Yoshimura teaches wherein forming the alignment mark comprised a plurality of grating structures in the substrate (Fig.5c (21c and 21d)).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshimura (WO 200167509 A) as applied to claims above, and further in view of Ridinger ('219).

In reference to claim 3, Yoshimura teaches the above method however fails to explicitly teach wherein the wafer has a diameter of 4, 8, or 12 inches. However, Ridinger teaches a wafer having a diameter in a range of 3 to 6 inches (Col.4, lines: 47-53). It would have been obvious to one of ordinary skill in the art to modify Yoshimura 's teachings to include a 4 inch semiconductor wafer as taught by Ridinger because Ridinger teaches that wafers with diameters between 3 and 6 inches are considered "standard" (Col.4, lines: 47-53).

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshimura (WO 200167509 A) as applied to claim 1 above, and further in view of Jang a et al ('137).

In reference to claim 9, Yoshimura teaches the limitations of claim 1, however fails to teach positioning the wafer in a photolithography stepper tool and reflecting a light off the alignment mark formed in the substrate to properly position the wafer for processing in the stepper tool as required by claim 9.

However, Jang teaches a similar method comprising:

Positioning the wafer in a photolithography stepper tool (Col.1, lines:40-45 and Col.7, lines: 15-20);

Reflecting a light off the alignment mark formed in the substrate to properly position the wafer for processing in the stepper tool (Col.1, lines: 40-45).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yoshimura to include the stepper tool and reflection step as disclosed by Jang because as Jang teaches, a photolithography stepper tool is an alignment tool which allows the alignment mark to perform aligning for subsequent processing (Col.7, lines; 10-20)

Response to Arguments

Applicant's arguments with respect to the above claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Laura M. Schillinger whose telephone number is (571) 272-1697. The examiner can normally be reached on M-T, R-F 7:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Laura M Schillinger
Primary Examiner
Art Unit 2813

08/21/06